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# Integration of Radiation-Hard Magnetic Random Access Memory with CMOS ICs

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## DISCLAIMER



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# Integration of Radiation-Hard Magnetic Random Access Memory With CMOS ICs

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## Abstract

The research undertaken in this LDRD-funded project addressed the joint development of magnetic material-based nonvolatile, radiation-hard memory cells with Sandia National Laboratory. Specifically, the goal of this project was to demonstrate the intrinsic radiation-hardness of Giant Magneto-Resistive (GMR) materials by depositing representative alloy combinations upon radiation-hardened silicon-based integrated circuits. All of the stated goals of the project were achieved successfully. The necessary films were successfully deposited upon typical integrated circuits; the materials retained their magnetic field response at the highest radiation doses; and a patterning approach was developed that did not degrade the as-fabricated properties of the underlying circuitry. These results establish the feasibility of building radiation-hard magnetic memory cells.

## Background

Ionizing radiation and electro-magnetic-pulse (EMP) effects are two of the major sources of bit upset in semiconductor memory systems. This difficulty stems from the fundamental mechanism by which semiconductor memories store information – accumulation of charge at a node in a capacitor or gate oxide well. Radiation and EMP events easily disrupt this charge state and the attendant memory information. Dynamic random access memory (DRAM) and static random access memory (SRAM) elements are particularly susceptible since the charge is stored on a capacitor. The other commonly used memory element (EE-PROM) is affected less than either DRAM or SRAM cells but has slow writing times, on the order of milliseconds, and it requires a second voltage source for its operation. Thus in circumstances requiring radiation and EMP tolerance there are serious disadvantages to using conventional semiconductor-based memory cells.

Recall that the basic storage requirements for a radiation-hard memory system include unlimited read-write cycles, long data retention lifetime, intrinsic radiation hardness, and material stability. It would also be desirable to have the memory elements to be readily fabricated, without exotic costly processes, thus lowering the cost of large-scale deployment. Since all of the currently available, large volume memory elements are based upon charge retention, many of these requirements are not met by semiconductor memory technology. One possible alternative that has been studied for about a decade is the use of ferroelectric materials. This class of materials, though, is known to suffer from two serious drawbacks: the number of useful read and write cycles is limited and data retention lifetime is too short for general applications.

A promising solution to these technical obstacles has arisen from research and development conducted in the magnetic hard disk drive industry. The use of magnetic materials in place of semiconductor materials for RAM has become feasible with the advent of this new class of magnetoresistive materials – the so-called Giant MagnetoResistive (GMR) multilayer stacks. These materials were initially investigated for use in magnetic sensors and have successfully replaced the older

generation of inductive read heads to achieve 5- to 10-fold increases in magnetic disk storage densities. The introduction of this technology for RAM development would have several natural advantages: non-volatility, intrinsic radiation hardness, manufacturing compatibility with existing integrated circuit technology, simpler processing steps than conventional DRAM fabrication, and higher bit densities than projected DRAM devices. The outstanding technical obstacle confronting MRAM development is the relatively slow access time. Introducing GMR materials with higher sensitivity can significantly reduce this access time.

The GMR effect intrinsically relies upon advances in thin layer deposition. Magnetic and non-magnetic metals are sandwiched in alternating layers to produce an anomalous magnetic field response. That is, a current is applied to the stack, either perpendicular or parallel to the layers and the magnetic field is switched from north to south. The resulting change in the resistance (magneto-resistive effect) can be quite large, on the order of 25 %. A schematic diagram of a typical GMR multi-layer stack is provided in Figure 1. These materials have completely displaced the previous conductive head technology. Hard drives using GMR-based heads ensure that the magnetic storage industry will continue its unprecedented growth, surpassing even that of the semiconductor market, for another five to seven years.

On the other hand, these devices have some significant problems when applied to memory storage. In particular, applying the current parallel to the layers leads to slow access times due to the unfavorable array geometry dictated by the current flow. Applying the current perpendicular to the multi-layer stack alleviates this problem but introduces two different difficulties. First, the use of conductive metals in a small stack leads to a very low impedance device raising serious signal-to-noise limitations. That is, low impedance leads to small voltage changes that will be hard to detect. Second, in this geometry, it then becomes necessary to have a switch to activate or deactivate each individual cell. The first difficulty has been overcome by the use of an insulating tunnel barrier, discussed below, while the second can, in principle, be controlled by placing a diode on the stack itself. One of the primary goals of the present research was to investigate low temperature laser annealing techniques to fabricate a diode on a metal layer.

Recent work at several industrial laboratories has demonstrated sufficiently large field sensitivity and high resistance by using an insulating layer to separate the active magnetic materials. Devices based upon this configuration would have natural process advantages in addition to their anticipated better performance. This class of device is known as a Magnetic Tunnel Junction (MTJ). A typical embodiment of an MTJ is shown in Figure 2. This stack operates in the following manner. When the magnetization directions of the magnetic materials are parallel (ferromagnetic), there is a relatively high probability that the electrons will tunnel through the insulating $Al_2O_3$ barrier. When the magnetization directions are anti-parallel (anti-ferromagnetic), the tunneling probability is low and, consequently, the resistance is high. This configuration, sketched in Figure 3, is especially suited to memory applications and intense development of these devices is being pursued at several industrial laboratories including IBM and Motorola.

An array of storage elements is required for high performance, non-volatile memory technology. In the conventional arrangement, the semiconductor memory cells are placed in a two-dimensional, x-y grid. Information is stored as bits of information inside “words” of data. Thus, to retrieve information, each bit of data in the chosen word is sequentially interrogated as shown in Figure 4. The physical layout of an individual cell is illustrated in Figure 5.

Thus to write data into a MTJ memory cell, the current is applied through the bit line and through the word line. The combined magnetic fields from these currents is sufficiently large to switch the magnetization direction of the soft ferromagnetic film of the tunnel junction. Conversely, to read the data from a tunnel junction cell, a sense current is applied to the stack. This sense current creates a voltage across the cell proportional to the resistance of the MTJ that allows the sense circuit to determine whether or not the cell is in a high or low resistance state, as dictated by the relative orientation of the magnetization in the different layers.

Briefly, the project entailed an investigation of the

The scaling experiments included features ranging from two micron radius to 0.35 micron radius. The three important process development steps involved ion beam etching, an image reversal process, and the development of a successful lift-off procedure. These last two steps Each of these steps is discussed briefly below.

Since the magnetic materials used in the multilayer stacks are restricted to the 3d transition metals, it is well known that these particular metals do not readily form volatile by-products in plasma reactions with any known chemically reacting gases. There is typically a large amount of re-deposited material near the structures being fabricated that will seriously compromise the field response of these structures. Thus it is essential to develop an etch process to remove this undesirable material. This step was successfully accomplished using a specially developed technique that selectively removed the magnetic materials using a photoresist layer as a mask in an Argon ion sputtering etch process.

The second technical fabrication challenge arose in the structure definition. The magnetic multilayers that were to be etched were very thin, usually less than 200 Angstroms thick. The electrical contacts to this thin stack consists of a thick metal layer that is several thousands of Angstroms thick. The process developed in this project involved sputtering the electrical lead material over the patterned GMR stack, followed by photolithographic definition of the lead structure. Ion beam etching is then used to remove the undesirable re-deposited material. The crucial point is to avoid over-etching of this material since the underlying, thin, GMR stack will be partially or totally removed during this step. To facilitate this overall procedure, an image reversal process, rather than a lift-off process, was used. The image reversal process requires several extra process steps but it had an important advantage since an additional mask was not required for the subsequent life-off process.

The final fabrication step involved a lift-off procedure applied to the image-reversed structure defined in the second step. The image reversal converted the pattern so that the electrical lead material could be deposited on the GMR contact area as well as on the resist where the lead material is superfluous. Dissolving the resist underlayer coating in acetone then removes this extraneous material from the wafer. This process had the singular advantage of avoiding an etch step to remove the electrical lead material and thus preserving the thin GMR stack buried beneath the leads. This lift-off step required a highly directional metal evaporation so that metal does not coat the resist sidewall which would prevent the acetone from dissolving the underlying resist.

Images of the structures produced after this sequence of process steps are shown in Figures 1, 2 and 3 that have photoresist remaining. In these figures, the electrical contact strips overlap the GMR multilayer stacks. Two different GMR stacks are displayed in Figures 1 and 2: 1.90 micron and 0.4 micron width. An expanded scale view is provided of the smaller structure in Figure 3. Although these structures are well-defined at this point in the processing, a final planarization step is necessary to complete the sample preparation. This remaining step unfortunately presented a severe difficulty for the smallest features. Overly aggressive chemical-mechanical planarization appeared to remove the smallest structures entirely from the wafer and this difficulty could not be overcome in the few months devoted to this project.

## Results

The largest fabricated features did indeed display a similar scaling response as that observed earlier but the failure of the small, less than 0.5 micron width devices, prevented the completion of a definitive experiment.. The magneto-resistive response was easily tracked for the larger structures and a large amount of information was gathered for these structures using a probe station. Oxidation of the samples was also an important limitation since direct contact with the electrical leads was difficult or impossible for some structures. The outstanding difficulty remains the planarization step. Alleviating this problem requires more development before it can be applied to these thin, small devices.

## Conclusion

It appears from the above experiments that the previous observations of enhanced response were correct and that partial oxidation of the patterned features is the primary cause. A successful process development sequence was developed that might be useful in the future for further investigation of spin-valve read-head structures or MRAM test structures. Further process development is still required to demonstrate that this effect can be usefully controlled to permit technological applications.

## Acknowledgments

The authors would like to thank Dr. M. Mao of LLNL for many useful discussions concerning the experimental layout and magnetic characterization of the samples. This work was performed at the Lawrence Livermore National Laboratory for the Department of Energy under contract W-7405-Eng-48.

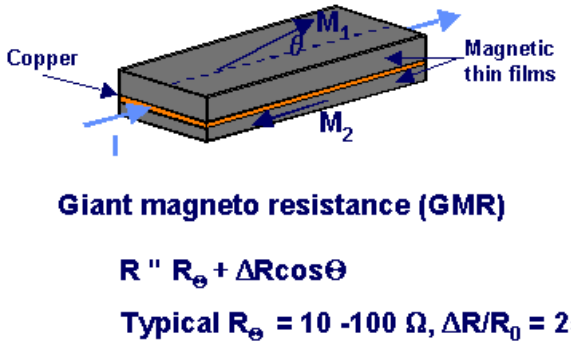



**Figure 1.** Principles of operation of giant-magnetoresistance (GMR) memory element. Current passes through a layer embedded between two magnetic materials in which the magnetization of the first layer occurs at an angle Θ to that of the second layer.

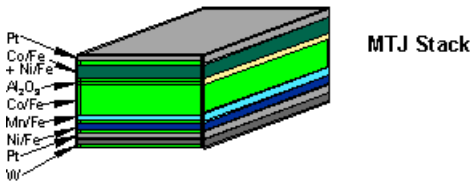
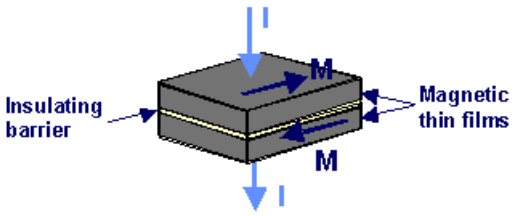



**Figure 2.** Material composition of the multilayer magnetic-tunnel-junction (MTJ) memory stack. The thin $Al_2O_3$ layer provides an insulating barrier between the two stacks of magnetic materials. Note that the magnetic materials used in the MTJ stack are the same as those used for magnetic tunnel junction technology.




**Magnetic tunnel junction (MTJ)**

**Typical** $R_0 = 1\Omega$, $\Delta R/R_0 = 25\%$

**Figure 3.** Principles of operation of magnetic-tunnel-junction (MTJ) memory element. The electrical of resistance of the memory element depends on the probability of electrons tunneling between the two layers, which is either larger or smaller depending on whether the magnetization M of the layers are parallel or anti-parallel.

**Circuit Configuration**

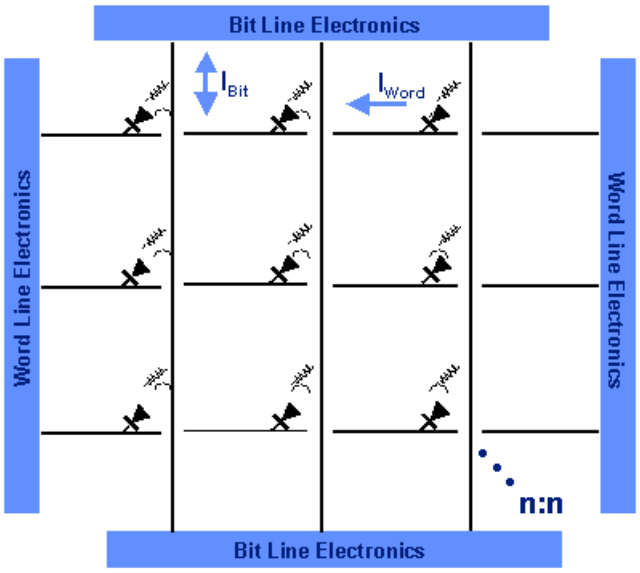



**Figure 5.** Schematic layout of a semiconductor memory based on magnetic tunnel junctions.

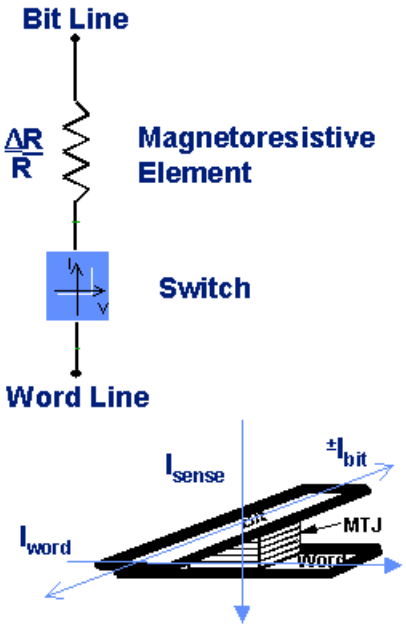



Figure 5. Schematic illustration of the circuit layout of the magnetic tunnel junction memory cell. An approach to fabricate the non-linear switching element has been developed by workers at Lawrence Livermore National Laboratory.

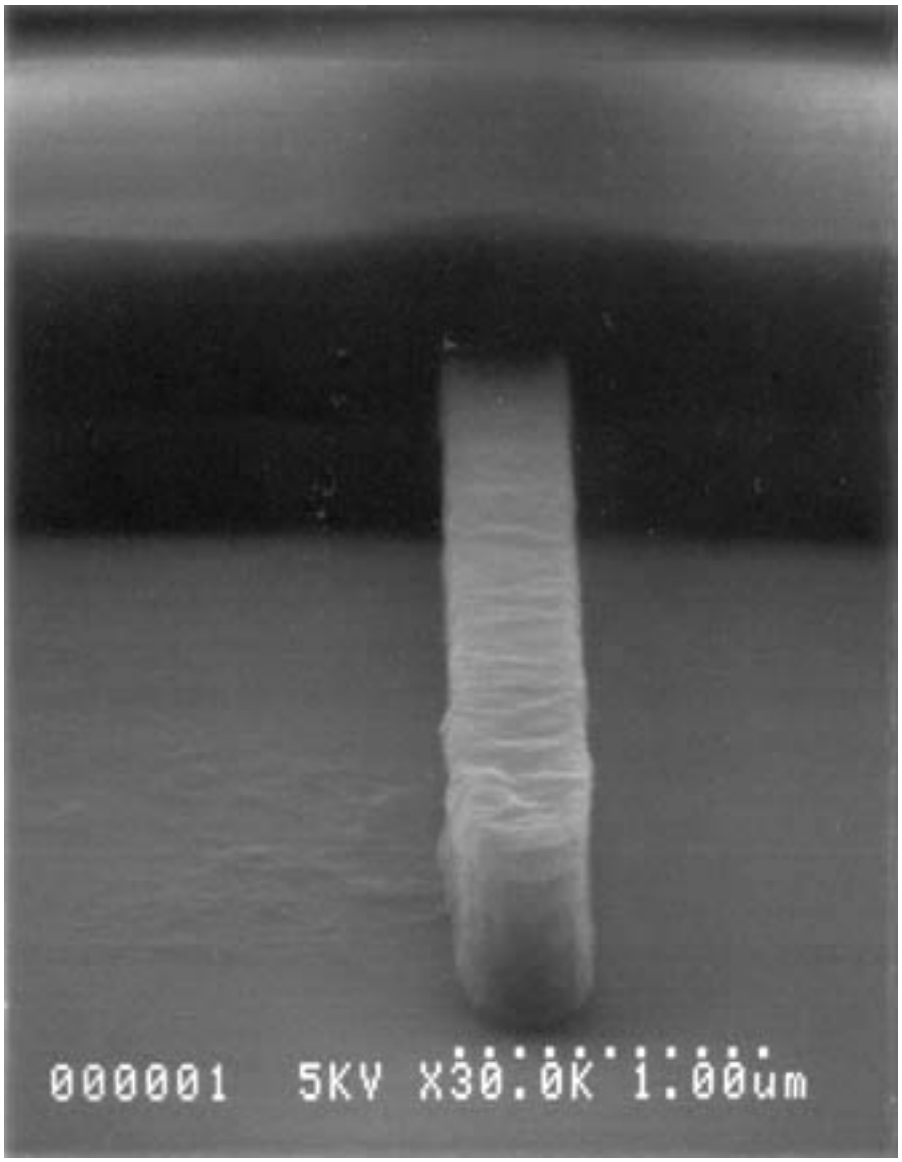



Figure 3